REMARKS/ARGUMENTS

Claims 1-20 are pending. Claims 1, 4, 9-11, and 13-15 have been amended. New claims 16-20 have been added. No new matter has been introduced. Applicants believe the claims comply with 35 U.S.C. § 112.

Claims 1-4, 6-10, and 12-15 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Saiki et al. (US 5,677,802).

Applicants respectfully submit that independent claim 1 is novel and patentable over Saiki et al. because, for instance, Saiki et al. does not teach or suggest a read clock control means for controlling the phase of said read clock signal in accordance with the phase of said read signal read by said magnetic head to correct the phase of said read clock signal if a phase shift between said read clock signal and said read signal exceeds a predefined value. As discussed in the specification at page 10, lines 6-9, correction of the phase by the read clock control means occurs if the phase shift exceeds a predefined value.

In contrast, Saiki et al. discloses phase correction by the VCO circuit. Nothing in Saiki et al. discloses or suggests making the phase correction if the phase shift exceeds a predefined value.

For at least the foregoing reasons, independent claim 1 and claims 2-4 and 6-8 depending therefrom are novel and patentable over Saiki et al.

Applicants respectfully assert that independent claim 9 is novel and patentable over Saiki et al. because, for instance, Saiki et al. does not teach or suggest a phase corrector configured to control said oscillator in accordance with the phase of said read signal, which is detected by said phase detector, in order to correct the phase of the read control signal generated by said oscillator if a phase shift between said read control signal and said read signal exceeds a predefined value. This is described in the specification at page 10, lines 21-23.

As discussed above, Saiki et al. discloses phase correction by the VCO circuit. Nothing in Saiki et al. discloses or suggests making the phase correction by a phase corrector if the phase shift exceeds a predefined value.

For at least the foregoing reasons, independent claim 9 and claims 10 and 12 depending therefrom are novel and patentable over Saiki et al.

Applicants respectfully contend that independent claim 13 is novel and patentable over Saiki et al. because, for instance, Saiki et al. fails to teach or suggest making corrections, if data is not successfully read due to a phase difference between said read clock signal and said read signal with said phase difference exceeding a predefined value, to adjust the phase of the read clock signal for the phase of the read signal.

As discussed above, Saiki et al. discloses phase correction by the VCO circuit. Nothing in Saiki et al. discloses or suggests making the phase correction if the phase shift exceeds a predefined value.

For at least the foregoing reasons, independent claim 13 and claims 14 and 15 depending therefrom are novel and patentable over Saiki et al.

Claims 5 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Saiki et al. in view of Muto et al. (US 5,436,770). The Examiner recognizes that Saiki et al. does not disclose that the storage means is a register provided for the read/write channel, and cites Muto et al. for the missing feature.

Applicants note, however, that Muto et al. does not cure the deficiencies of Saiki et al. in that Muto et al. also fails to teach or suggest a read clock control means for controlling the phase of said read clock signal in accordance with the phase of said read signal read by said magnetic head to correct the phase of said read clock signal if a phase shift between said read clock signal and said read signal exceeds a predefined value, as recited in claim 1 from which claim 5 depends; and a phase corrector configured to control said oscillator in accordance with the phase of said read signal, which is detected by said phase detector, in order to correct the phase of the read control signal generated by said oscillator if a phase shift between said read control signal and said read signal exceeds a predefined value, as recited in claim 9 from which claim 11 depends.

For at least the foregoing reasons, claims 5 and 11 are patentable over Saiki et al. and Muto et al.

New claims 16-20 depend from independent claims 1, 9, and 13, and are submitted to be patentable as being directed to additional feature not taught or suggested in the references, as well as by being dependent from allowable claims 1, 9, and 13, respectively. For example, claim 16 recites that the read clock control means is stable when the phase shift between the read clock signal and the read signal is not greater than the

predefined value, making PLL (phase-locked loop) based phase adjustments possible. See, e.g., specification at page 11, lines 15-16. Claim 17 recites that data is not successfully read by the data read means with the phase shift exceeding the predefined value. See, e.g., specification at page 4, lines 14-20. Claim 18 recites that the oscillator is stable when the phase shift between the read control signal and the read signal is not greater than the predefined value, making PLL (phase-locked loop) based phase adjustments by the phase detector and the oscillator possible. Claim 19 recites that if the phase difference is not greater than the predefined value, the phase detector and the oscillator are configured to performing PLL (phase-locked loop) based phase adjustments to the phase of the read clock signal to match the phase of the read signal. Claim 20 recites that the method further comprises, if the phase difference is not greater than the predefined value, performing PLL (phase-locked loop) based phase adjustments to the phase of the read clock signal to match the phase of the read signal. See, e.g., specification at page 9, line 23 to page 10, line 1; page 10, lines 19-21; and page 11, lines 19-20. These feature are absent from the cited references.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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